PATENT

Remarks

By this amendment claims 1 and 16 have been amended. Claims 1 through 16 are pending, no new matter has been entered, and reconsideration thereof is requested.

Claim Rejections - 35 U.S.C. § 103

The Examiner rejected Claims 1,2,5,8 and 9 under 35 U.S.C.§ 103(a) as being unpatentable over Crafts (U.S. Patent No. 6,064,588) and Iizuka et al (U.S. Patent No. 4,641,165). The Examiner indicates that Crafts shows most aspects of the instant invention including first and second transfer devices and differential storage capacitor. The Examiner points out that Crafts does not show the primary capacitance of the storage capacitor being at least approximately 5 times the inherent capacitance of the said capacitance, but mentioned Iizuka, et al. teaches how to make a primary capacitor to be at least approximately 5 times the inherent capacitance. The Examiner concludes it would have been obvious to make the primary capacitance to be approximately 5 times the inherent capacitance.

The Applicants respectfully believe that the references do not show, or suggest, the present invention. Further, Iizuka et al. do not teach a differential capacitance at least 5 times the inherent capacitances since Iizuka does not incorporate a differential capacitor. It is not clear as to what would serve as a differential node in Iizuka et al., namely the substrate, brings with it a very large capacitance to the storage node. No motivation appears in the cited references to produce the claimed invention, consider if one were to re-wire the capacitor of Iizuka et al. in a differential manner, it would not present at least 5 times the inherent capacitance without further invention.

Thus, the works of Crafts and Iizuka et al. taken together require further invention to identify a low-capacitance means of wiring the second capacitor node of Iizuka et al. differentially.

Moreover, the Examiner bases the rejections of claims 1, 2, 5, 8 and 9 on Crafts (US6,064,588) in view of Iizuka (US 4,641,165). The Examiner points out that "Crafts does not explicitly show the primary capaticance of the storage being at least approximately 5 times the inherent capacitance" and goes on to argue that it would have been obvious to make it so. However, a closer inspection of the invention of Crafts reveals that is is not reasonable possible for the work of Crafts to achieve such a ratio. The reason for this is that Crafts teaches away from our invention by providing an explicit connection, 63, between the capacitors that are in series, and furthermore, this connection links all of the pairs of capacitors to a common node. This connection explicitly defeats the purpose of our invention as any charge loss in any one capacitor to a surrounding electrical node will discharge that particular capacitance with a return current through the connection, 63, thereby defeating the cancellation that is enjoyed by our invention. Our inventive structure is topologically distinct from that of Crafts, and uniquely possesses our claimed ability to prevent differential charge loss. In the Crafts structure, any charge lost in any one capacitor is not offset in its differential complement, since the common lines connecting the return paths of the storage capacitors in Crafts will provide the discharge path. Even if Crafts leaves the return line "floating," the aggregate of all of the cells tied to this one node (63) act exactly as an inherent capacitance and are in aggregate much greater than the differential

capacitance; hence the storage capacitance must, in fact, be less than that of the inherent capacitance in the invention of Crafts. This difference underscores the novelty of our invention.

Iizuka provides an entirely different approach to charge storage from both our invention and that of Crafts. Iizuka uses a circuit topology distinct from Crafts, and application of the low-capacitance node to Crafts memory cell would make result in inherent capacitance that is still larger than the storage capacitance by virtue of the common connection in Crafts (63). Thus the teaching of Iizuka together with that of Crafts fails to achieve the desired result of our invention. Iizuka can keep the inherent capacitance low by virtue of the resistor isolation, "R" in Fig. 11, which when applied to the work of Crafts becomes defeated by the essential connection "63". Hence, the combination of these two works distinctly fails to lead to our invention.

Furthermore, neither work identifies the use of fully-depleted transfer devices that prevents differential charge loss which are the subject of Claims 1,2,5,8 and 9 in order to enable the capacitance goals recited therein.

Based on the foregoing, it is respectfully submitted that Claims 1,2,5,8 and 9 are not obvious under 35 U.S.C.§103(a).

The Examiner rejected claims 3 and 4 under 35 U.S.C. 103(a) as being unpatentable over Crafts and Iizuka et al., as applied to Claim 1 above, and further in view of Tashiro (U.S. Patent No. 5,241,211).

The Examiner indicated that Crafts and Iizuka et al. show most aspects of the instant invention except for the SOI substrate. Tashiro teaches (e.g. Column 1, Lines 14 to 23) to use SOI substrates to reduce parasitic capacitances. The Examiner believes that it would have been obvious to a person of ordinary skill in the art at the time of invention to use an SOI substrate as taught by Tashiro in the device of Crafts and Iizuka et al. to reduce parasitic capacitances.

The Examiner further rejects our claims 3 and 4 citing Tashiro (US5,241,211) over Crafts and Iizuka. While Tahiro does teach use of an SOI substrate which does result in a lower capacitance, there is still a component of inherent capacitance proportional to the area of the structure in planar structures such as taught by Tashiro, which limits the ability to reduce the inherent capacitance. Once again, application of the structure of Tashiro (planar SOI) to the storage cells of Crafts and Iizuka in any combination, still fails to teach or suggest our invention as pointed out earlier.

The Applicants also wish to point out that Iizuka et al. and Crafts do not suggest the invention of Claim 1. Nor does Tashiro teach or suggest the use of an SOI substrate for a U-groove structure.

Tashiro does not address the issues of providing low intrinsic (isolation) capacitance for a differential capacitor. Thus claims 3 and 4 are not made obvious by Tashiro, even taken with Crafts and Iizuka et al.

Based on the foregoing, it is submitted that claims 3 and 4 are not obvious under 35 U.S.C.§ 103(a).

The Examiner rejected claims 6,7,and 10 to 16 under 35 U.S.C.§103(a) as being unpatentable over Crafts and Iizuka et al., as applied to Claim 1 above, and further in view of Choi et al. (DRC 2000).

The Examiner indicated that Crafts and Iizuka et al. show most aspects of the instant invention except for the features of the transfer devices and the storage capacitor disposed on rails of semiconductor material. Choi et al. teach (e.g. Figure 1) to form semiconductor devices using semiconductor rails to reduce parasitic capacitance and resistance. The Examiner believes it would have been obvious to a person or ordinary skill in the art at the time of invention to form semiconductor devices using semiconductor rails as taught by Choi et al. in the device of Crafts and Iizuka et al. to reduce parasitic capacitance and resistance.

The Applicants point out again that Iizuka et al. and Crafts do not suggest the invention of Claim 1 or 16. Nor does Choi et al. teach or suggest the use of ultra-thin-body SOI to form and FET. They do not contribute to the use of "rails" nor differential capacitor configurations. They further teach away from rails in that they describe planar thin silicon with the body plane parallel to the wafer substrate, in contrast to our invention where the body planes are explicitly perpendicular to the wafer substrate in order to provide low parasitic capacitance to the substrate which prevents differential charge loss.

Finally, adding the work of Choi, et al. (DRC 2000) fails to teach our invention since Choi brings none of the features of inherent capacitance vs storage capacitance, and only teaches a basic FinFET structure.

Based on the foregoing, it is submitted that Claims 6, 7, and 10 to 16 are not obvious under 35 U.S.C.§103(a).

Conclusion

Based on the foregoing, it is respectfully submitted that all the claims active in the subject patent application are in condition for allowance and that the application may be passed to issuance.

The Examiner is urged to call the undersigned at the number listed below if, in the Examiner's opinion, such a phone conference would aid in furthering the prosecution of this application.

Respectfully submitted,

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